Claims

1. A storage device comprising:

a memory for storing data ;and

a circuit having a data input, a control input, and a data output;

wherein the circuit provides data input from the data input to the memory in accordance with a control signal from the control input to store data provided to the data input in the memory or to output data stored in the memory to the data output.

2. The storage device according to claim 1, wherein the circuit inputs a command from the data input to the memory in accordance with the control signal to store the data in the memory or to output data stored in the memory to the data output.

3. The storage device according to claim 1, wherein the circuit provides an address input from the data input to the memory in accordance with a control signal from the control input to store data provided to the data input at the address in the memory or to output data at the address in the memory to the data output.

4. The storage device according to claim 3, wherein the circuit has ports for providing the data and the address to the memory and a data bus for transferring the data from the data input to one of the ports by the control signal of the control input.

5. The storage device according to claim 4, wherein the circuit has another data bus for transferring the data from the one of the ports to the data output by the control signal.

6. The storage device according to claim 4, wherein the ports comprise flip-flops for holding and outputting the data from the data bus to the memory by the control signal, and buffers for outputting the data from the memory to the data bus by the control signal.

7. The storage device according to claim 4, wherein selection and read/write of the ports is controlled by bits input to the control input.

8. The storage device according to claim 4, wherein the circuit inputs a command for selection and read/write of the ports from the data input by the control signal of the control input.

9. The storage device according to claim 3, wherein the circuit inputs part of the address from the data input to set the part to selected bit of a held address that is modified by the part, and provides the modified address to the memory.

10. The storage device according to claim 1, wherein the circuit inputs part of the data from the data input to set the part to selected bit of held data that is modified by the part, and provides the modified data to the memory.

11. The storage device according to claim 1, wherein the circuit has a readable port set to a status for identification and control of access to the memory.

12. The storage device according to claim 11, further comprising, a switch connected to the port for setting the status.

13. The storage device according to claim 1, further comprising, another memory for storing data to which the circuit provides the data.

14. The storage device according to claim 1, wherein data for identification in a predetermined header area is written in the memory.

15. The storage device according to claim 1, wherein the memory has a mode in which the data are successively output from the memory.

16. The storage device according to claim 1, wherein the memory is one of a ROM, a static memory, an EEPROM, a dynamic memory, a flash memory, and a ferroelectics memory.

17. The storage device according to claim 1, wherein the data input inputs parallel data and the data output outputs parallel data.

18. The storage device according to claim 1, further comprising, a

connector connected to the data input, the data output, and the control input, and for supplying power to the storage device.

19. A method for access to a storage device having a data input, a control input, a data output, and a memory for storing data, wherein the storage device inputs data from the data input, and provides the data to the memory in accordance with a control signal from the control input to store the data in the memory or to output data in the memory to the data output, comprising:

providing data to the data input to output the data to the memory; and

providing a first control signal to the control input to store the data into the memory.

20. The method according to claim 19, wherein the storage device inputs a command from the data input, and provides the data to the memory in accordance with the command to store the data in the memory or to output data in the memory to the data output, comprising:

providing the command to the data input;

providing data to the data input to output the data to the memory; and

providing the first control signal to the control input to store the data into the memory in accordance with the command.

21. The method according to claim 19, wherein the storage device inputs an address from the data input, and provides the data to the memory in accordance with a control signal from the control input to store the data at the provided address in the memory or to output data at the address in the memory to the data output, comprising:

providing an address to the data input to output the address to the memory;

providing data to the data input to output the data to the memory; and

providing the first control signal to the control input to store the data at the address into the memory.

22. The method according to claim 21, further comprising:

providing an address to the data input to set the address of memory; and

providing a second control signal to the control input to output the data at the address in the memory to the data output.

23. The method according to claim 21, further comprising, providing part of the address to set the part to selected bits of an address held in the storage device for modifying the address and output the modified address to the memory.

24. The method according to claim 19, wherein the data output outputs the data transfered between the data input and the memory, comprising:

inputting the transferred data from the data output to confirm whether the data is correct.

25. The method according to claim 19, wherein the memory has a mode in which the data are successively output from the memory, and the method further comprises turning control status of the memory by providing signals to the storage device such that the memory operates in the mode.

26. The method according to claim 19, wherein the storage device has a readable port set to a status for identification of an access type of the memory, comprising, reading the status to identify access type of the memory.

27. The method according to claim 19, wherein the data input inputs parallel data and the data output outputs parallel data.

28. An apparatus having (1) an interface for data exchange from and to a storage device having a data input, a control input, a data output, and a memory for storing data, wherein the storage device inputs data from the data input, provides the data to the memory in accordance with a control signal from the control input to store the data memory or to output data in the memory to the data output, and (2) a connector for connecting the data input, a data output and the control input to the interface and supplying power to the storage device, wherein the apparatus provides the control signal to the control input from the interface, and the data to the data input from the interface to store the data in the memory or to output data in the memory to the data output.

29. The apparatus according to claim 28, wherein the storage device inputs a command from the data input, provides the data to the memory in accordance with the command to store the data in the memory or to output data in the memory to the data output, and the apparatus provides the control signal to the control input

from the interface, and the command and the data to the data input from the interface, to store the data in the memory or to output data in the memory to the data output.

30. The apparatus according to claim 28, wherein the storage device inputs an address from the data input, provides the address to the memory in accordance with a control signal from the control input to store the data at the provided address in the memory or to output data at the address in the memory to the data output, and the apparatus provides the control signal to the control input from the interface, and the address and the data to the data input from the interface, to store the data at the address in the memory or to output data at the address in the memory to the data output.

31. The apparatus according to claim 30, wherein the apparatus provides part of the address to the data input to set the part to selected bits of an address held in the storage device for modifying the address and output the modified address to the memory.

32. The apparatus according to claim 28, wherein the memory has a mode in which the data are successively output from the memory, and the apparatus provides signals to the storage device such that the memory operates in the mode by turning control status of the memory.

33. The apparatus according to claim 28, wherein the apparatus exchanges data among a plurality of the storage devices, through the interface, and the apparatus further comprises connectors for connecting the data inputs of the storage devices to the interface and connecting the data inputs to each other.

34. The apparatus according to claim 28, wherein the data output outputs data transferred between the data input and the memory, and the apparatus inputs the transferred data from the data output to confirm whether the data is correct.

35. The apparatus according to claim 28, wherein the storage device has a readable port set to a status for identification and control of access to the memory, and the apparatus reads the status from the interface to identify access type of the memory.

36. The apparatus according to claim 28, wherein supplying power to the storage device is controlled.

37. The apparatus according to claim 28, wherein the data input inputs parallel data which the interface provides to the data input and the data output outputs parallel data which the interface inputs from the data output.

38. The apparatus according to claim 28, further comprising, a microcontroller in which the interface is provided.